IN THE SPECIFICATION:

Please amend paragraph **[0001]** as follows:

**[0001]** This application is a continuation of U.S. Patent Application Serial No. 08/985,588, filed on December 5, 1997, now U.S. Patent No. 5,953,621, issued September 14, 1999, which is a divisional patent application of U.S. Patent Application Serial No. 08/823,609, filed on March 25, 1997, now U.S. Patent No. 6,097,076, issued August 1, 2000, both of which are incorporated herein by reference.

Please amend paragraph **[0008]** as follows:

**[0008]** An active area may be formed within semiconductor substrate 12 immediately beneath pad oxide 14, and adjacent isolation material 48. A problem that is inherent in such non-planarity of fill material within an isolation trench is that corners 62 may leave the active area of semiconductor substrate 12 exposed. As such, isolation material 48 will not prevent layers formed thereon from contacting the active area of semiconductor substrate 12 at corners 62. Contact of this sort is detrimental in that it causes charge and current leakage. Isolation material 48 is also unable to prevent unwanted thermal oxide encroachment through corners 62 into the active area of semiconductor substrate 12.

Please amend paragraph **[0009]** as follows:

**[0009]** What is needed is a method of forming an isolation trench, where subsequent etching of fill material within the isolation trench of such method prevents overlying layers from having contact with an adjacent active area, and prevents unwanted thermal oxide encroachment into the active area. What is also needed is a method of forming an isolation trench wherein etching or planarizing such as by chemical mechanical chemical-mechanical planarization (CMP) of isolation trench materials is accomplished without forming a recess at the intersection of the fill material in the isolation trench and the material of the active area within the semiconductor substrate.

Please amend paragraph **[0013]** as follows:

**[0013]** A third dielectric layer is formed substantially conformably over the spacer and the first dielectric layer so as to substantially fill the isolation trench. Topographical reduction of the third dielectric layer follows, preferably so as to planarize the third dielectric layer for example by chemical mechanical layer, for example, by chemical-mechanical planarizing (CMP), by dry etchback, or by a combination thereof.

Please amend paragraph **[0014]** as follows:

**[0014]** The topographical reduction of the third dielectric layer may also be carried out as a single etchback step that sequentially removes superficial portions of the third dielectric layer that extend out of the isolation trench. The single etchback also removes portions of the remaining spacer, and removes substantially all of the remaining portions of the first dielectric layer. Preferably, the single etchback will use an etch recipe that is more selective to the third dielectric layer and the spacer than to the remaining portions of the first dielectric layer. The single etchback uses an etch recipe having a selectivity that will preferably leave a raised portion of the third dielectric layer extending above the isolation trench while removing substantially all remaining portions of the first dielectric layer. The resulting structure can be described as having the shape of a nail as viewed in a direction that is substantially orthogonal to the cross section cross-section of a word line in association therewith.

Please amend paragraph **[0025]** as follows:

**[0025]** FIGS. 5A and 5B illustrate further processing of the structure structures depicted, respectively, in FIGS. 4A and 4B, in which the insulation film has been etched to form a spacer, a simultaneous or serial etch has formed an isolation trench, thermal oxidation or deposition within the isolation trench has formed an insulation liner therein, and wherein an optional ion implantation has formed a doped region at the bottom of the isolation trench.

Please amend paragraph **[0026]** as follows:

**[0026]** FIGS. 6A and 6B illustrate further processing of the structure structures depicted, respectively, in FIGS. 5A and 5B, in which an isolation film has been deposited over the spacer, the isolation trench within the isolation trench liner, and the nitride island.

Please amend paragraph **[0027]** as follows:

**[0027]** FIGS. 7A and 7B illustrate further processing of the structure structures depicted, respectively, in FIGS. 6A and 6B, wherein a planarization process has formed a first upper surface made up of the nitride island, the spacer, and the isolation film, all being substantially co-planar on the first upper surface.

Please amend paragraph **[0028]** as follows:

**[0028]** FIG. 8A illustrates further processing of the structure structures depicted in FIGS. 7A or 9A, wherein the semiconductor substrate has been implanted with ions, and wherein the isolation film, optionally the pad oxide layer, the insulation liner, and the spacer have fused to form a unitary isolation structure.

Please amend paragraph **[0029]** as follows:

**[0029]** FIG. 8B illustrates optional further processing of the structure structures depicted in FIG. 6B, wherein an etching process using an etch recipe that is slightly selective to oxide over nitride, has etched back the isolation film, the nitride island, and the spacer to expose the polysilicon island, and has formed a filled isolation trench which, when viewed in a direction that is substantially orthogonal to the cross section cross-section of the depicted word line, has the shape of a nail.

Please amend paragraph **[0030]** as follows:

**[0030]** FIG. 9A illustrates optional further processing of the structure structures depicted in FIG. 6A or in FIG. 7A, wherein an etch-selective recipe that is slightly selective to

oxide over nitride has formed a filled isolation trench which, when viewed in cross section, cross-section has the shape of a nail.

Please amend paragraph **[0031]** as follows:

**[0031]** FIG. 9B illustrates further processing of the structure structures depicted in either FIGS. 7B or 8B wherein the semiconductor substrate has been implanted with ions, and wherein the isolation film, optionally the pad oxide layer, the insulation liner, and the spacer have been fused to form a filled isolation trench.

Please amend paragraph **[0036]** as follows:

**[0036]** FIG. 4A illustrates further processing of the structure depicted in FIG. 3A, wherein an insulation film 26 has been deposited upon insulator island 22 and exposed portions of pad oxide 14. Insulation film 26 can be an oxide such as silicon dioxide, and can be formed for example by decomposition of tetraethyl ortho silicate orthosilicate (TEOS). Insulation film 26 may also be formed by a plasma enhanced chemical vapor deposition (PECVD) process so as to deposit a nitride layer such as Si.sub.3N.sub.4 $Si_3N_4$ or equivalent. When insulation film 26 is a nitride layer, insulator island 22 would be selected to be composed of a substantially different material, such as an oxide. Formation of substantially different materials between insulator island 22 and insulation film 26 facilitate selective etchback or selective mechanical planarization such as chemical-mechanical polishing (CMP) in the inventive method of forming an isolation trench.

Please amend paragraph **[0037]** as follows:

**[0037]** Following deposition of insulation film 26, a spacer etch and an isolation trench etch are carried out. The spacer etch and the isolation trench etch can be carried out with a single etch recipe that is selective to insulation film 26. Alternatively, the spacer etch and the isolation trench etch can be carried out with two etch recipes. As such, the first etch etches insulation film 26 in a spacer etch that forms a spacer 28 seen in FIG. 5A. The second etch, or isolation trench etch, has an etch recipe that is selective to spacer 28 and insulator island 22, and

anisotropically etches an isolation trench 32 having ~~a side wall~~ sidewall 50 in semiconductor substrate 12.

Please amend paragraph **[0041]** as follows:

**[0041]** Insulation liner 30 may be substantially composed of a nitride such as ~~Si.sub.3N.sub.4,~~ $Si_3N_4$, or an equivalent, and can be selectively formed upon sidewall 50 of isolation trench 32. When semiconductor substrate 12 immediately adjacent to isolation trench 32 is a doped monocrystalline silicon that forms, for example, an active area for a transistor source/drain region, oxidation is avoided therein by insulation liner 30. Insulation liner is preferably substantially composed of ~~Si.sub.3N.sub.4~~ $Si_3N_4$ or a non-stoichiometric variant ~~which~~ that seals sidewall 50 so as to prevent encroachment of oxide into semiconductor substrate 12.

Please amend paragraph **[0042]** as follows:

**[0042]** Following formation of insulation liner 30, ion implantation is optionally carried out to form a doped trench bottom 34 at the bottom of isolation trench 32. For example, if semiconductor wafer 10 comprises an N-doped silicon substrate, implantation of P-doping materials at the bottom of isolation trench 32 will form a P-doped trench bottom 34. Ion implantation may be carried out in a field implantation mode. If a complementary metal oxide semiconductor (CMOS) is being fabricated, however, masking of ~~complimentary~~ complementary regions of semiconductor substrate 12 is required in order to achieve the differential doping thereof. For an N-doped silicon substrate, a high breakdown voltage may be achieved by P-doping. A low breakdown voltage may be achieved by N-doping, and an intermediate breakdown voltage may be achieved by no doping. Because the present invention relates to formation of isolation trenches, P-doping in an N-well region, or N-doping in a P-well region are preferred.

Please amend paragraph **[0047]** as follows:

**[0047]** It is preferable, at some point in fabrication of the isolation trench, to densify the fill material of the isolation trench. Densification is desirable because it helps to prevent separation of materials in contact with the fill material. As seen in FIG. 6A, densification will prevent isolation film 36 from separating at interfaces with spacer 28, pad oxide ~~layer~~ 14, and insulation liner 30. It is preferable to perform densification of isolation film 36 immediately following its deposition. Depending upon the specific application, however, densification may be carried out at other stages of the process. For example, densification of isolation film 36 by rapid thermal processing (RTP) may make either etchback or CMP more difficult. As such, it is preferable to densify later in the fabrication process, such as after planarizing or etchback processing.

Please amend paragraph **[0048]** as follows:

**[0048]** FIG. 7A illustrates a subsequent step of formation of the isolation trench wherein insulator island 22, spacer 28, and isolation film 36 are planarized to a common co-planar first upper surface 38. First upper surface 38 will preferably be formed by a CMP or etchback process. Preferably, planarization will ~~remove to~~ remove isolation film 36 slightly faster than insulator island 22, such as by a factor of about one half. A first preferred selectivity of an etch recipe used in the inventive method is in the range of about 1:1 to about 2:1, wherein isolation film 36 is removed faster as compared to insulator ~~island.~~ island 22. A more preferred selectivity is in the range of about 1.3:1 to about 1.7:1. A most preferred selectivity is about 1.5:1. Planarization also requires the etch recipe to remove spacer 28 slightly faster than insulator island 22. ~~Preferably~~ Preferably, spacer 28 and ~~insulator~~ isolation film 36 are made from the same material such that the etch will be substantially uniform as to the selectivity thereof with respect to spacer 28 and isolation film 36 over insulator island 22.

Please amend paragraph **[0049]** as follows:

**[0049]** First upper surface 38 is illustrated as being substantially planar in FIG. 7A. It will be appreciated by one of ordinary skill in the art that first upper surface 38 will form a

non-planar profile or topography depending upon the selectivity of the etch recipe or of the chemical used in a planarization technique such as CMP. For example, where reduced island 52 is formed from a nitride material and isolation film 36 is formed from an oxide material, first upper surface 38 would undulate as viewed in ~~cross-section~~ cross-section with more prominent structures being the result of an etch or planarization technique more selective thereto.

Please amend paragraph **[0052]** as follows:

**[0052]** Phantom lines 60 in FIG. 8A illustrate remnants of pad oxide ~~layer~~ 14, insulation liner 30, and spacer 28 as they are optionally thermally fused with isolation film 36 to form isolation structure 48. Isolation structure 48, illustrated in FIG. 8A, comprises a trench portion and a flange portion which together, when viewed in ~~cross-section,~~ cross-section, form the shape of a nail.

Please amend paragraph **[0053]** as follows:

**[0053]** The trench portion of isolation structure 48 is substantially composed of portions of isolation film 36 and insulation liner 30. The trench portion intersects the flange portion at a second upper surface 40 of semiconductor substrate 12 as seen in FIG. 8A. The trench portion also has two sidewalls 50. FIG. 8A shows that the trench portion is substantially parallel to a third upper surface 42 and sidewalls 50. The flange portion is integral with the trench portion and is substantially composed of portions of pad oxide ~~layer~~ 14, spacer 28, and isolation film 36. The flange portion has a lowest region at second upper surface 40 where the flange portion intersects the trench portion. The flange portion extends above second upper surface 40 to third upper surface 42 seen in FIG. 8A. Upper surfaces 40, 42 are substantially orthogonal to two flange sidewalls 64 and sidewall 50. The flange portion is substantially orthogonal in orientation to the trench portion. The flange portion may also include a gate oxide layer 44 after gate oxide layer 44 is grown.

Please amend paragraph **[0057]** as follows:

**[0057]** Gate oxide layer 44 is formed upon second upper surface 40 after pad oxide 14 has been removed to form portions of third upper surface 42. The entirety of third upper surface 42 includes head 54 of isolation structure 48 as it extends above gate oxide layer 44 ~~and gate oxide layer 44~~.

Please amend paragraph **[0058]** as follows:

**[0058]** In a variation of the first embodiment of the present invention, the structure illustrated in FIG. 6A is planarized by use of a single etchback process. The single etchback uses an etch recipe that has a different selectivity for insulator island 22 than for isolation film 36. In this alternative embodiment, spacer 28, ~~dielectric~~ isolation film 36, and pad oxide 14 are composed of substantially the same material. Insulator island 22 has a composition different from that of isolation film 36. For example, isolation film 36 and spacer 28 are composed of ~~SiO.sub.2,~~ $SiO_2$, and insulator island 22 is composed of silicon nitride.

Please amend paragraph **[0061]** as follows:

**[0061]** A starting structure for an example of a second embodiment of the present invention is illustrated in FIG. 2B. In FIG. 2B, pad oxide ~~layer~~ 14 is grown upon semiconductor substrate 12 and a polysilicon layer 18 is deposited upon pad oxide ~~layer~~ 14. This embodiment of the present invention parallels the processing steps of the first embodiment with the additional processing that takes into account the use of polysilicon layer 18.

Please amend paragraph **[0062]** as follows:

**[0062]** FIG. 3B illustrates etching through nitride layer 16 and polysilicon layer 18 to stop on pad oxide ~~layer~~ 14. The etch creates both an insulator island 22 and a polysilicon island 24 formed, respectively, from nitride layer 16 and polysilicon layer 18.

Please amend paragraph **[0063]** as follows:

**[0063]** FIG. 4B illustrates further processing of the structure depicted in FIG. 3B, wherein insulation film 26 has been deposited upon insulator island 22, laterally exposed portions of polysilicon island 24, and exposed portions of pad oxide ~~layer~~ 14. Following deposition of insulation film 26, a spacer etch and an isolation trench etch are carried out similarly to the spacer etch and isolation trench etch carried out upon semiconductor structure 10 illustrated in FIG. 5A.

Please amend paragraph **[0064]** as follows:

**[0064]** FIG. 5B illustrates the results of both the spacer etch and the isolation trench etch and optional implantation of isolation trench 32 to form ~~doped well~~ trench bottom 34 analogous to doped trench bottom 34 illustrated in FIG. 5A. Formation of insulation liner 30 within isolation trench 32 preferentially precedes implantation to form ~~doped~~ P-doped trench bottom 34. Following optional implantation of doping ions, full or partial removal of spacer 28 may optionally be performed as set forth above with respect to the first embodiment of the invention.

Please amend paragraph **[0068]** as follows:

**[0068]** To form the structure seen in FIG. 9B, semiconductor structures 10 of FIGS. 7B or 8B are subjected to implantation of semiconductor substrate 12 with ions. Semiconductor structure 10 is then subjected to a heat treatment so as to fuse together isolation film 36, optional pad oxide ~~layer~~ 14, insulation liner ~~60,~~ 30, and spacer 28 into an integral filled isolation trench.

Please amend paragraph **[0069]** as follows:

**[0069]** Subsequent to the process illustrated in FIGS. 6A-8A and 6B-9B a final thermal treatment, or subsequent thermal treatments, can be performed. Heat treatment may cause isolation structure 48 to be wider proximal to third upper surface 42 than proximal to doped trench bottom 34. When so shaped, an unoxidized portion of the active area of semiconductor substrate 12 that forms sidewall 50 would have a trapezoidal shape when viewed in ~~cross section,~~

cross-section, where the widest portion is second upper surface 40 and the narrowest portion is at doped trench bottom 34. Where a trapezoidal shape of the trench portion causes unwanted encroachment into the active area of semiconductor substrate 12, the optional formation of insulation liner 30 from a nitride material or equivalent is used to act as an oxidation barrier for sidewall 50. Semiconductor structure 10 is illustrated in FIG. 9B as being implanted by doping ions, as depicted with ~~downwardly-directed~~ downwardly directed arrows. Following a preferred implantation, thermal processing may be carried out in order to achieve dopant diffusion near upper surface 42b of implanted ions residing within semiconductor substrate 12. Due to head 54 extending onto semiconductor substrate 12, a doping concentration gradient can be seen between the active area 53a and the active area 53b. The starting and stopping point of the doping concentration gradient in relation to flange sidewalls 64 will depend upon the duration and temperature of a thermal treatment.

Please amend paragraph **[0070]** as follows:

**[0070]** The present invention may be carried out wherein spacer 28 and isolation film 36 are substantially composed of the same oxide material, and insulator island 22 is substantially ~~composes~~ composed of a nitride composition. Other compositions may be chosen wherein etch selectivity or CMP selectivity slightly favors insulator island 22 over both spacer 28 and isolation film 36. The specific selection of materials will depend upon the application during fabrication of the desired isolation trench.